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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/702,372	11/05/2003	Ming-Dou Ker	JC-7897-DIV	8473

23900 7590 11/29/2005

J C PATENTS, INC.
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EXAMINER	
STARK, JARRETT J	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AAK

Office Action Summary	Application No.	Applicant(s)	
	10/702,372	KER ET AL.	
	Examiner	Art Unit	
	Jarrett J. Stark	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *39-42 and 46-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *39-42 and 46-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. 10060743.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 39 rejected under 35 U.S.C. 102(b) as being anticipated by Voldman et al. (US 6,015,993).

Regarding claim 39, Voldman teaches a method of forming a non-gate diode of a SOI, comprising:

providing a SOI with a substrate (Voldman, Figs. 7), an insulating layer (Voldman, Figs. 7, element 156) and a silicon layer (Voldman, Figs. 7, element 154) sequentially stacked together,

forming a pair of isolating structures (Voldman, Fig. 7, elements 126) in the silicon layer, so as to define a well region (Voldman, Fig. 7, elements 152) there between;

forming a first type doped region and a second type doped region in the well region and adjacent to the isolating structures (Voldman, Fig. 7, elements 162 & 164) .

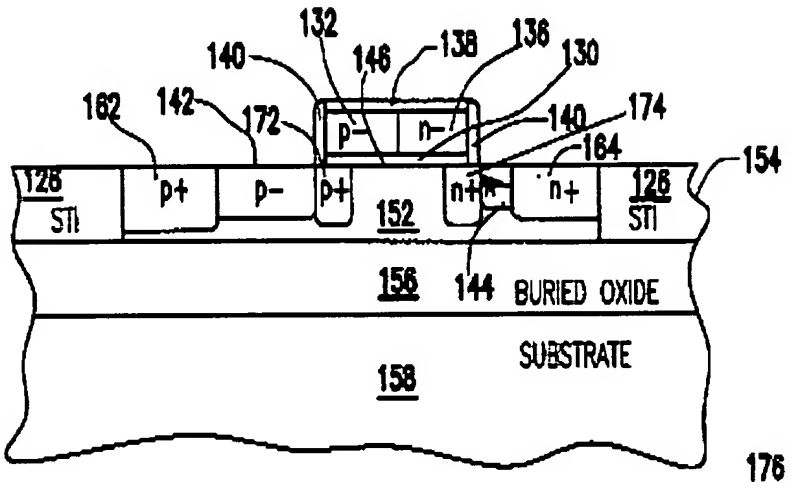

FIG.7

Regarding claim 40, Voldaman teaches the method according to claim 39, wherin the first type and second type doped regions are implanted with P-type and N-type ions, respectively (Voldaman, Fig. 7, elements 162 & 164).

Regarding claim 41, Voldaman teaches the method according to claim 39, wherein the well region is lightly implanted with a P-type ion (Voldaman, Fig. 7, elements 142).

Regarding claim 42, Voldaman teaches the method according to claim 39, wherein the well region is lightly implanted with an N-type ion (Voldaman, Fig. 7, elements 144).

Regarding claim 46, Voldaman teaches a method of forming a non-gate diode in a CMOS process, comprising:

Providing a substrate (Voldaman, Fig. 7, elements 156) having a well region therein (Voldaman, Fig. 7, elements 152);

Forming a pair of blocking isolation structures in the substrate (Voldaman, Fig. 7, elements 126);

Forming a first type-doped region (Voldaman, Fig. 7, elements 162) located in the well region and between the blocking isolation structure, and

Forming a pair of second type doped regions (Voldaman, Fig. 7, elements 144 & 164) located in the well region and respectively adjacent to the blocking isolation structure (Voldaman, Fig. 7, elements 126), wherein each second type doped region is separated from the first type doped region by the well (Voldaman, Fig. 7, elements 152).

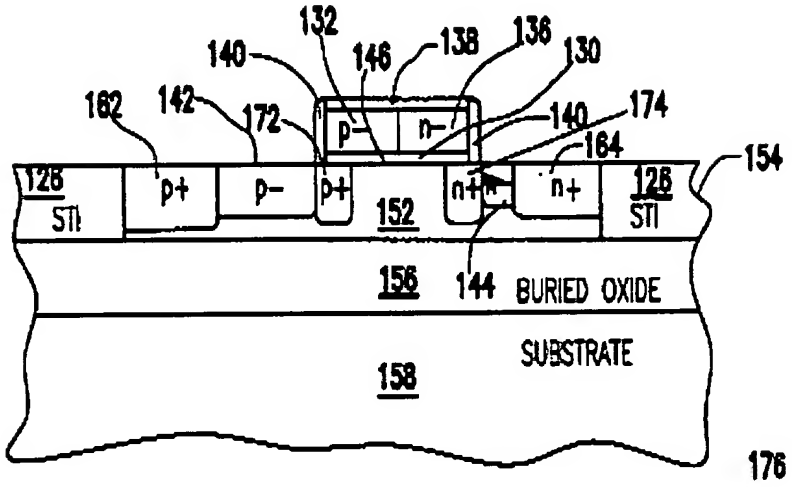

FIG.7

Regarding claim 47, Voldaman teaches the method according to claim 46, wherin the first type doped region and the second type doped region are implanted with P-type and N-type ions respectively (Voldaman, Fig. 7, elements 162 & 164).

Regarding claim 48, Voldaman teaches method according to claim 46, wherein the well region is lightly implanted with a P-type ion (Voldaman, Fig. 7, elements 142).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jarrett J. Stark whose telephone number is (571) 272-6005. The examiner can normally be reached on Monday - Thursday 6:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571)272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JJS
November 22, 2005

W. DAVID COLEMAN
PRIMARY EXAMINER